IN THE CLAIMS

We claim:

1. A semiconductor wafer comprising:

a plurality of semiconductor integrated circuits separated by a plurality of scribe lines; and

a plurality of dummy features formed in said scribe lines.

2. The semiconductor wafer of claim 1 wherein said dummy features and active features in said scribe lines create a feature density in said scribe lines which is substantially similar to the feature density in the portion of the semiconductor integrated circuit adjacent to said scribe line.

3. The semiconductor wafer of claim 1 wherein said density of features in said scribe line is within ± 10% of the density of features in the portion of the integrated circuit adjacent to said scribe line.

4. A level of an integrated circuit comprising:

a core area, said core area having a first density of features; and

a peripheral area, said peripheral area having a second density of features wherein said second density is substantially similar to said first density.

5. The level of an integrated circuit of claim 4 wherein said second density is within ± 10% of said first density.

6. A level of an integrated circuit comprising:

a first area having a first plurality of features having a first density; and

a second area adjacent to said first area, said second area having a plurality of dummy features having a density substantially similar to said first density.

7. The level of claim 6 wherein said first density is approximately 50%.

8. The integrated circuit of claim 4 wherein said dummy features have substantially the same pitch as the features in said first area.

9. The level of an integrated circuit of claim 6 wherein said dummy features have substantially the same shape and spacing as said features in said first area.

10. The level of claim 6 wherein said shape and spacing of said dummy features are within 30% of said shape and spacing of said first plurality of features.

11. A method of generating a layout in an integrated circuit comprising:

generating a first layout of a level of active features, said first layout having a first area and a second area adjacent to said first area wherein the first area has a first density of active features and wherein said second area has a second density of active features; and

increasing or decreasing the size of said active features in said second area so that the density of said active features in said second area is similar to said density of active features in said first area.

12. The method of claim 11 wherein said first area and said second area have an area of approximately 25 μm^2.

13. The method of claim 11 wherein said active features comprise conductive lines or plugs.

14. An integrated circuit comprising:

a plurality of levels of features wherein at least one of said levels of features consists of a plurality of 25 μm^2 areas having a plurality of features therein wherein the average density of said feature in each of said plurality of 25 μm^2 areas are substantially similar.

15. The integrated circuit of claim 14 wherein the average density is approximately 50%.

16. The integrated circuit of claim 15 wherein said features in each of said plurality of active areas has substantially the same pitch and separation.

17. A method of generating a level of an integrated circuit comprising:

generating a first layout of a level of an integrated circuit having a first area of active features with a first density and a second area of active features with a second density, wherein said first density is greater than said second density;

generating a second layout of said level of said integrated circuits by adding dummy features to said second area to make the density of said features in said second area similar to the density of features in said first area;

generating a photolithographic mask for said second layout;

using said photolithographic mask to pattern a conductive film into active features and dummy features;

depositing a dielectric film over and between said active features and said dummy features; and

chemically mechanically polishing said dielectric film until said dielectric is substantially planar.

18. The method of claim 17 wherein said chemical mechanical polishing is continued until said active and dummy features are exposed.

19. A method of generating a level of an integrated circuit comprising:

generating a first layout of a level of an integrated circuit having a first area of active features with a first density and a second area of active features with a second density, wherein said first density is greater than said second density;

generating a second layout of said level of said integrated circuits by adding dummy features to said second area to make the density of said features in said second area similar to the density of features in said first area;

generating a photolithographic mask from second layout;

using said mask to pattern a dielectric film into a patterned dielectric film having active feature openings and dummy feature openings;

depositing a conductive film over and between said active feature openings and said dummy feature openings; and

chemically mechanically polishing said conductive film until said conductive film is substantially planar with the top of said pattern dielectric layer.